Course code	Course Name	L-T-P-Credits	Year of Introduction
IT201	Digital System Design	3-1-0-4	2016

Prerequisite : Nil

Course Objectives

1. To impart an understanding of the basic concepts of Boolean algebra and digital circuit design.
2. To provide familiarity with the design and implementation of different types of practically used combinational and sequential circuits.
3. To provide an introduction to Hardware Description Language
4. To expose the students to basics of arithmetic algorithms

Syllabus

Introduction to Number Systems, Boolean Algebra, Canonical Forms, Logic Gates, Digital Circuit Design - Combination Logic Circuit Design, Sequential Circuit Design, Registers, Counter, Memory modules, Programmable Logical Arrays, Hardware Description Language for Circuit Design, Case study with VHDL, Arithmetic algorithms

Expected Outcomes

Student will be able to:-

1. Apply the basic concepts of Boolean algebra for the simplification and implementation of logic functions using suitable gates namely NAND, NOR etc.
2. Design simple Combinational Circuits such as Adders, Subtractors, Code Convertors, Decoders, Multiplexers, Magnitude Comparators etc.
3. Design Sequential Circuits such as different types of Counters, Shift Registers, Serial Adders, Sequence Generators.
4. Use Hardware Description Language for describing simple logic circuits.
5. Apply algorithms for addition/subtraction operations on Binary, BCD and Floating Point Numbers.

Text Books:

1. Mano M. M., *Digital Logic & Computer Design*, 4/e, Pearson Education, 2013.
2. Charles H Roth ,Jr, Lizy Kurian John, *Digital System Design using VHDL*,2/e, Cengage Learning

References:

1. Tokheim R. L., *Digital Electronics Principles and Applications*, 7/e, Tata McGraw Hill, 2007.
2. Mano M. M. and M. D Ciletti, *Digital Design*, 4/e, Pearson Education, 2008.
3. Rajaraman V. and T. Radhakrishnan, *An Introduction to Digital Computer Design*, 5/e, Prentice Hall India Private Limited, 2012.
4. Leach D, Malvino A P, Saha G, *Digital Principles and Applications, 8/e, McGraw Hill Education, 2015.*
5. Floyd T. L., *Digital Fundamentals*, 10/e, Pearson Education, 2009
6. M. Morris Mano, *Computer System Architecture*, 3/e, Pearson Education, 2007.
7. Harris D. M. and, S. L. Harris, Digital *Design and Computer Architecture*, 2/e, Morgan Kaufmann Publishers, 2013

COURSE PLAN			
Module	**Contents**	**Contact Hours**	**Sem. Exam Marks**
I	Number systems – Decimal, Binary, Octal and Hexadecimal – conversion from one system to another –representation of negative numbers – representation of BCD numbers – character representation – character coding schemes – ASCII – EBCDIC etc Addition, subtraction, multiplication and division of binary numbers (no algorithms). Addition and subtraction of BCD, Octal and Hexadecimal numbers Representation of floating point numbers – precision –addition, subtraction, multiplication and division of floating point numbers	10	**15%**
II	Introduction — Postulates of Boolean algebra – Canonical and Standard Forms — logic functions and gates Methods of minimization of logic functions — Karnaugh map method and Quine- McClusky method Product-of-Sums Simplification — Don't-Care Conditions.	09	**15%**
III	Combinational Logic: combinational Circuits and design procedure — binary adder and subtractor — multi—level NAND and NOR circuits — Exclusive-OR and Equivalence Functions. Implementation of combination logic: parallel adder, carry look ahead adder, BCD adder, code converter, magnitude comparator, decoder, multiplexer, demultiplexer, parity generator.	09	**15%**
IV	Sequential logic circuits: latches and flip-flops – edge triggering and level-triggering — RS, JK, D and T flipflops — race condition — master-slave flip-flop. Clocked sequential circuits: state diagram — state reduction and assignment — design with state equations	07	**15%**
V	Registers: registers with parallel load - shift registers universal shift registers – application: serial adder.	08	**20%**

	Counters: asynchronous counters — binary and BCD ripple counters — timing sequences — synchronous counters — up-down counter, BCD counter, Johnson counter, Ring counter		
VI	Memory and Programmable Logic: Random-Access Memory (RAM)—Memory Decoding—Error Detection and Correction — Read only Memory (ROM), Programmable Logic Array (PLA). *HDL:* fundamentals, combinational logic, adder, multiplexer. Case Study : Implementation of 4-bit adder and 4-bit by 4-bit multiplier using VHDL Arithmetic algorithms: Algorithms for addition and subtraction of binary and BCD numbers, algorithms for floating point addition and subtraction , Booth's Algorithm	**10**	**20%**

QUESTION PAPER PATTERN (End semester examination)

Maximum Marks : 100 Exam Duration: 3 hours

Part A –(Modules I and II) 2 out of 3 questions (uniformly covering the two modules) are to be answered. Each question carries 15 marks and can have a maximum of 4 sub divisions

Part B – (Modules III and IV) 2 out of 3 questions (uniformly covering the two modules) are to be answered. Each question carries 15 marks and can have a maximum of 4 sub divisions

Part C – (Modules V and VI) 2 out of 3 questions (uniformly covering the two modules) are to be answered. Each question carries 20 marks and can have a maximum of 4 sub divisions